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Attorney's Docket No.: INTEL 10559-165001 / P8249

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Bryan R. White
Serial No. : 09/676,844
Filed : September 29, 2000
Title : SHARED TRANSLATION ADDRESS CACHING

Art Unit : 2676
Examiner : Mackly Moonestime

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Technology Center 2600

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO FINAL OFFICE ACTION OF JUNE 11, 2003

ASSIGNEE: INTEL CORPORATION

In reply to the Final Office Action of June 11, 2003, Applicant submits the following remarks. Each remark of the applicant below is preceded by a quotation of the related comments of the Examiner, shown in bold small type.

2. The following is a quotation of 35 U. S. C. 103(a)which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims l-3, 7-9 and 13 are rejected under 35 U. S. C. 103(a)as being unpatentable over Fisher et al (US Patent No. 6,480,200)in view of Ajanovic et al (US Patent No. 6,374,3 17).

4. Fisher et al was cited in the last office action.

5. As per claims 1 and 13, Fisher et al substantially disclosed the invention as claimed, including a memory controller hub comprising: a cache adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data (col. 1, lines 58-61) and available to an external graphics controller hub to store graphics data (Fig. 1, Item No. 18). Fisher et al did not explicitly disclose that the controller hub includes an internal graphics subsystem adapted to perform graphics operations on data. However, Ajanovic et al disclosed a memory controller which includes an internal graphics subsystem adapted to perform graphics operations on data (Fig. Items No. 110, 113; col 3, lines 45-47). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have implemented the memory controller hub of Ajanovic et al into the system of Fisher et al because doing so would provide a more flexible and expandable graphics system by allowing the memory controller to accommodate a plurality of interfaces such as graphics interface and interface controller.

6. As per claim 7, Fisher et al substantially disclosed the invention as claimed, including a CPU (Fig. 1, Item No. 10); a display device (Fig. 1, Item No. 24); a system memory adapted to store video data and non-video data; and a memory controller hub coupled to the CPU (Fig. 1, Item No. 12)and coupled to the system memory (Fig. 1, Item No. 14), the memory controller hub comprising: a cache adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data (col. 1, lines 58-61)and available to the memory controller hub to store graphics data (Fig. 1, Item No. 18). Fisher et al did not explicitly disclose that the controller hub includes an internal graphics subsystem adapted to perform graphics operations on data. However, Ajanovic et al disclosed a memory controller which includes an internal graphics subsystem adapted to perform graphics operations on data (Fig. Items No. 110, 113; col 3, lines 45-47). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have implemented the memory controller hub of Ajanovic et al into the system of Fisher et al because doing so would provide a more flexible